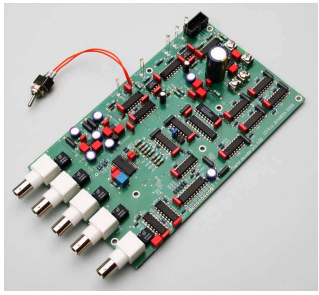
DIGITAL DECODER PRO for NON-OVERSAMPLING DAC



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FEATURES

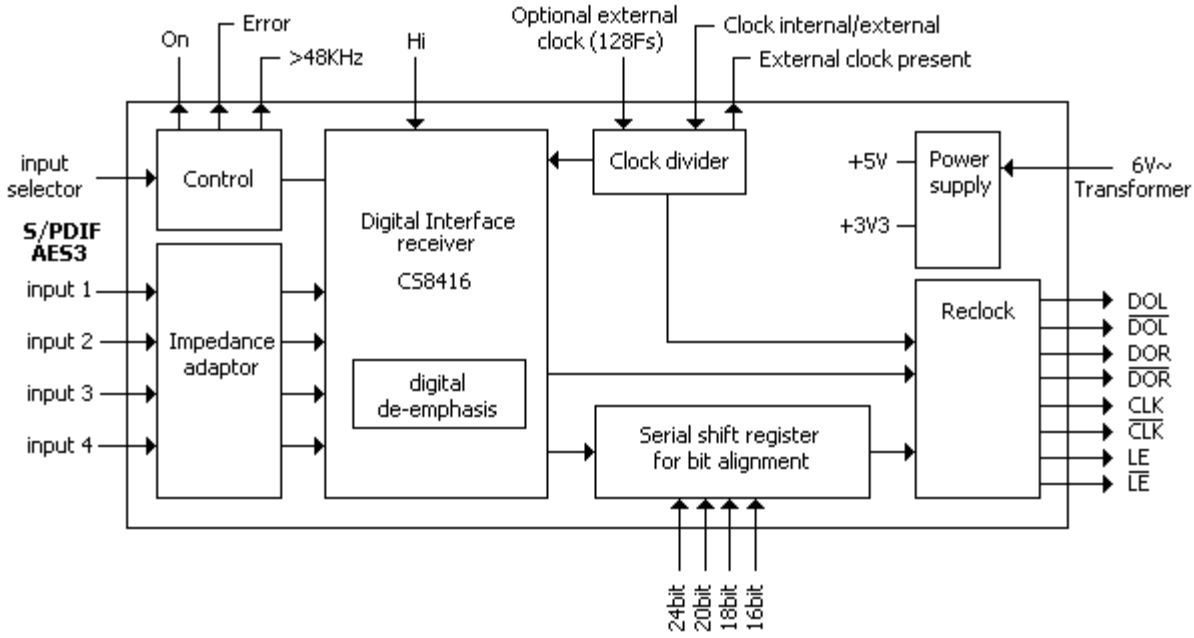
- **FOUR DIGITAL INPUTS**
  S/PDIF, AES3
- **RCA, BNC or XLR input connector**
- **ACCEPT 16, 18, 20, 24 BIT DAC CHIP**
- **32K TO 192KHz**
- **NO OVERSAMPLING**
  no digital filter
- **OPTIONAL CLOCK INPUT: 128FS**
  to minimize jitter
- **DIGITAL TRANSFORMER INPUT**
- **INCLUDE CS8416 DIR RECEIVER**
  with digital de-emphasis
- **DIRECT INTERFACE TO**
  PCM1704
  PCM1702
  PCM56…
- **LOW NOISE REGULATORS**
  LT1763
- **BOARD SIZE : 114mm X 190mm**

DESCRIPTION

The DIGITAL DECODER PRO is the first stage of a non-oversampling digital to analog converter. It allows a direct interface to a standard 16 to 24 bit DAC chip. The board incorporates four S/PDIF, AES3 (AES/EBU) digital inputs.

The optional input clock allows for very low jitter operation.

The board incorporates 4 SMD ICs, the others are standard DIL. High speed ICs are of the 74AC family with symmetrical output impedance and balanced propagation delay. Each high speed IC is decoupled with individual ferrite bead and Wima© capacitors FKP2 polypropylene film and foil or MKS2, MKS02 metalized polyester.



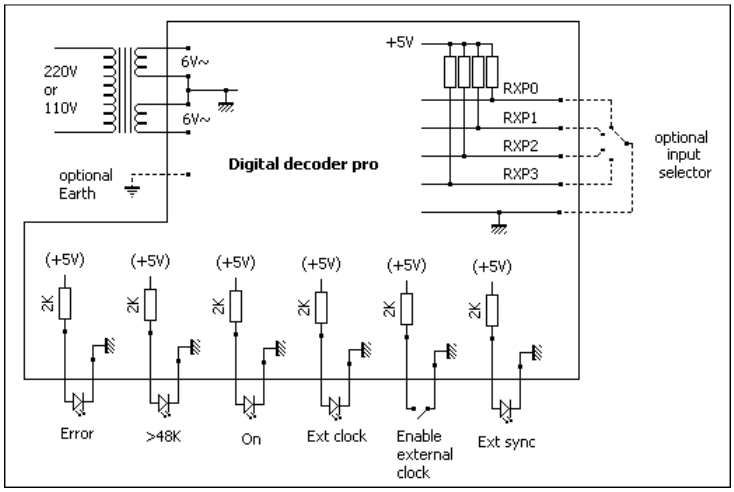
SPECIFICATIONS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input sensitivity	RXP0, RXP1, RXP2, RXP3	0.15	0.5	5	Vp-p
	External clock			5	Vp-p
Load input [(1)]	S/PDIF – BNC (RXPn)	50	75		Ohm
	S/PDIF – RCA (RXPn)		75		Ohm
	AES3 – XLR (RXPn)		110		Ohm
	External clock		75		Ohm
Input signal	Resolution	16		24	Bit
	Sample frequency	30		200	KHz
	Number of channels		2		
	Audio format		PCM		
Power supply requirements	Before regulation		6		V~
			200		mA
Digital output	CLK, LE, DOL, DOR.		5		V
Output jitter[(2)]	Without external clock		200		ps RMS
Output frequency	32KHz < fs < 192KHz				
LE	LE = fs	32		192	KHz
CLK	CLK = 64xFs	2.048		12.288[(3)]	MHz
Data output format	16, 18, 20, 24 bits MSB first, right aligned, left and right channel aligned.				
Led indicator					
ON	Power ON				
Error	PLL unlock				
>48 KHz	input fs is greater than 48KHz				
Ext clock	external clock present				
Ext sync	synch on external clock				

(1) Load input can be adjusted at any value. Each input has its own load. You can mix 75 and 110 Ohm loads.

(2) According to CS8416 datasheets, typical RMS cycle-to-cycle jitter.

(3) 12.288 MHz can exceed max clock frequency permitted by some DAC chip like PCM56.



External connection (digital data not shown)

AUDIO DATA INTERFACE

BASIC OPERATION

The DIGITAL DECODER PRO is the first stage of a non oversampling stereo digital audio converter system. DIGITAL DECODER PRO allows bit resolution selection and data alignment for direct wiring to a DAC chip. The DIGITAL DECODER PRO input accepts S/PDIF or AES3 encoded digital data.

INPUT

Each input connector accepts BNC, RCA or XLR. All inputs are isolated by a differential transformer. Input impedance can be individually adjusted for 75 Ohm, 110 Ohm or 50 Ohm. See figure 1.

DIGITAL DECODER PRO integrates four inputs (RXP0, RXP1, RXP2, RXP3). The input selector allows switching to desired input. Link desired input selector pin to GND to select desired input. Without pin to GND, RXP3 is selected. See figure 2.

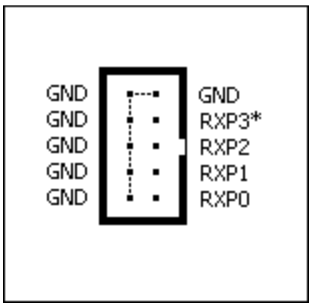


FIGURE 2 – Top view of input selector

DATA RESOLUTION

Data resolution is adjusted by a four position jumper. Data resolution must match with the DAC chip. Data resolution can be adjusted for 16, 18, 20 or 24 bits.

DATA FORMAT

All data output is TTL 5V. The data format at the DOR/DOL output is Binary Two's Complement, right aligned, with the most significant bit (MSB) being first. The bit clock (CLK) is used to shift data into the DAC chip. LE pin indicates the end of valid data. For convenience all outputs are provided with normal and reverse state: CLK, $\overline{\text{CLK}}$, LE, $\overline{\text{LE}}$, DOL, $\overline{\text{DOL}}$, DOR and $\overline{\text{DOR}}$.

See figure 3 and 4.

BIT CLOCK RATE

Table II shows LE and CLK pulse for normalized sample frequency (fs). CLK = 64 x fs.

fs	LE	CLK
44.1 KHz	44.1 KHz	2.8224 MHz
48 KHz	48 KHz	3.072 MHz
96 KHz	96 KHz	6.144 MHz
192 KHz	192KHz	12.288 MHz[(3)]

TABLE II

[(3)]12.288 MHz can exceed the max clock frequency permitted by some DAC chips like PCM56.

ERROR REPORT

An internal NE555 reports all errors on Error LED for one second. Errors are reported if a parity, bi-phase, confidence or PLL lock error occurs during current sample. See NVERR function on CS8416 datasheets.

RECLOCKING

All data output are re-clocked with 128 fs clock frequency. This frequency comes from CS8416 when used as an internal clock. When an external clock is present and enabled, data are re-clocked with the external clock.

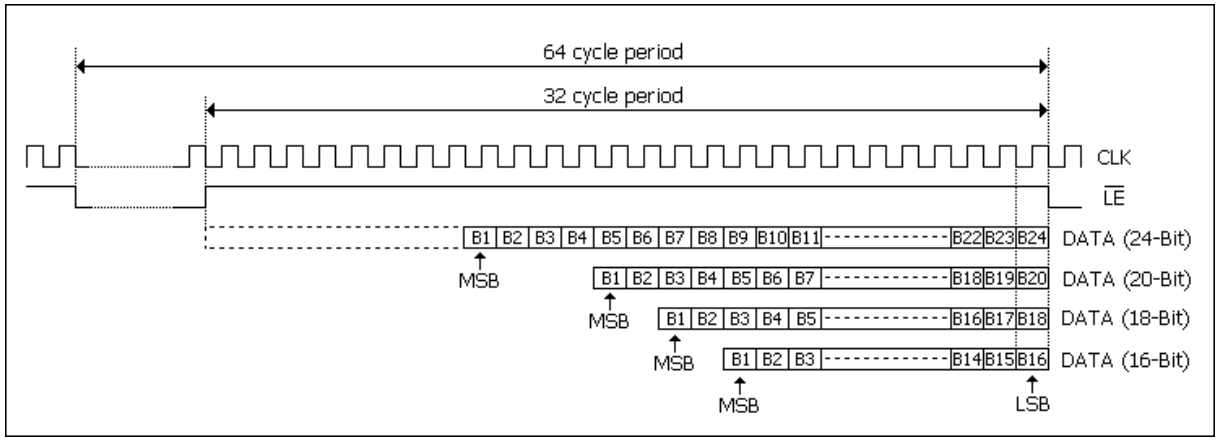


FIGURE 3. – Relation between CLK, LE et DATA. DATA is DOR or DOL.

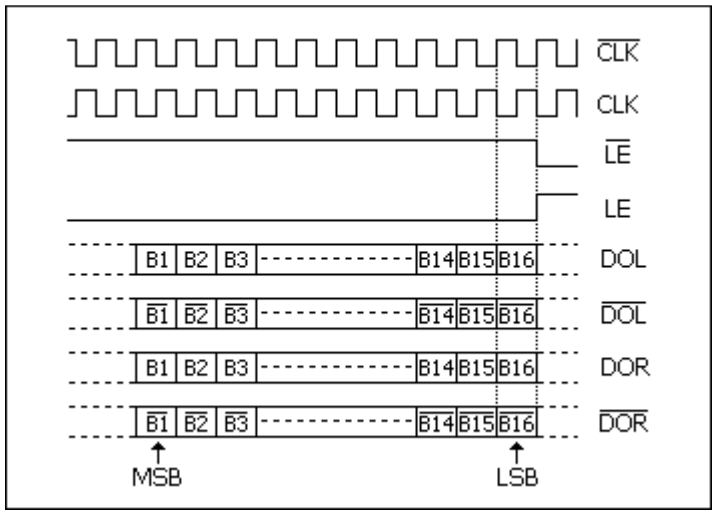


FIGURE 4 – Relation between all data output. Diagram shows 16 bit data output. For 18, 20 and 24 bit, timing alignment is the same. LE occurs at the end of LSB to be compliant with right data alignment.

THEORY OF OPERATION

AVOID REFLEXION

Best practice to minimize jitter is to keep constant 75 Ohm impedance on all digital links: source connector, digital cable and source receiver.

So, the 75 Ohm input connector is recommended; it keeps very low reflection on data transfer. Reflections cause PLL *moving*.

DAC CHIPS

DIGITAL DECODER PRO can be combined with various DAC chips. Table III gives a non exhaustive list of ICs.

Texas Instruments Burr-Brown	**Analog Devices**
PCM56	AD766
PCM1702	AD1851
PCM1704	AD1856
	AD1861
	AD1866
Obsolete	Obsolete
PCM58	AD1860
PCM61	AD1862
PCM63	AD1864
PCM1700	AD1865
	AD1868

Table III

EXTERNAL CLOCK

DIGITAL DECODER PRO integrates an external clock input. This external clock can be used to obtain minimum jitter and best audio rendering. The same clock might be used to synchronize digital source and DIGITAL DECODER PRO. Clock frequency on external clock input must be 128 x fs (sampling frequency).

When a signal clock is present, ***Ext clock*** Led is on. ***Clock ON*** switch permits to switching to internal or external clock. Each switches ON/OFF performs one second reset state on CS8416, during this phase there is no signal output. The ***Ext sync*** LED is ON when DIGITAL DECODER PRO is synchronized by the external clock.
There is no match verification between digital audio input sampling frequency and the external clock. For correct operation, the external clock must be 128 x input sampling frequency.

For best performance, jitter on external clock must be as low as possible.

When external sync is active, CS8416 works in slave mode; else CS8416 works in master mode.

BALANCED OUTPUT

Re-clocking is performed with high speed 74AC574 chip with symmetrical output impedance and balanced propagation delay.

PLL WORKING

Closing **HI** pin allows CS8416 working in higher phase detector update rate. In this mode, PLL could not lock on 192 KHz digital input signal.

If **HI** pin is open (recommended operation), CS8416 works in normal phase detector update rate.

HI pin must be switched before power on or reset operation. See CS8416 datasheets for more information.

TYPICAL APPLICATION EXAMPLES

Figure 5 shows typical connections for standard application using two 24 bit DAC without an external clock.

Figure 6 shows a sample application for external clock. CD player and DIGITAL DECODER PRO are synchronized with a same crystal.

Figure 7 shows typical connections using four DAC chips for balanced current output.

Figure 8 shows single channel circuit connections for a typical DAC board using a PCM1704 24 bit DAC chip, open loop discrete I/V converter and first order low pass filter.

ABOUT UNFILTERED DAC

Listening to unfiltered NOS DAC is not recommended. Humans don't hear high frequencies produced by unfiltered NOS DAC but can feel it. First impression, digital audio signal seems very sweat, detailed, analog and natural. Nothing seems digital at all!

After a period (1mn to 3 hours), you fell an important auditory tiredness. It is like someone putting needles in your tympanum! This unpleasant sensation is due to excessive high frequency radiation (16 KHz – 20 KHz).

Putting a first order low pass filter is enough to cut off this unpleasant feeling and keeping natural sound.

ABOUT HIGH ORDER LOW PASS FILTER

High order low pass filter (third order or more) destroys tonal balance. Phase shift introduced by this filter destroys sound coherence. Prefer low order low pas filter.

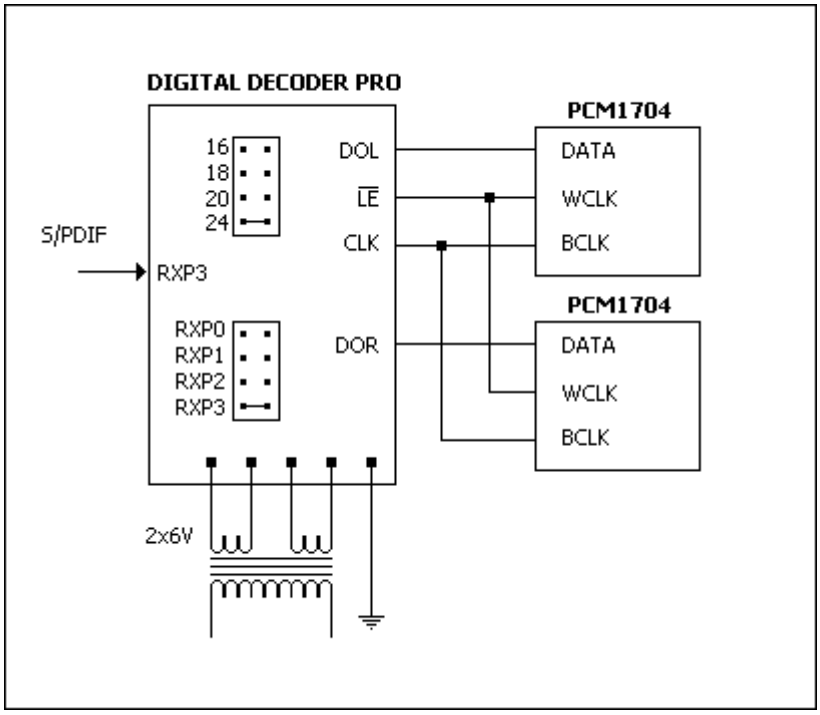


FIGURE 5 – Typical connection.

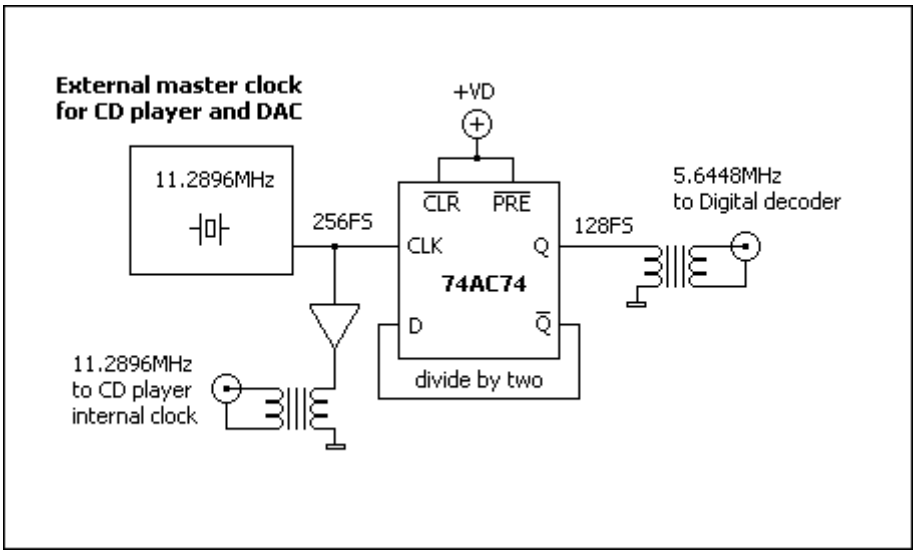


FIGURE 6 – Sample application for external clock and CD using 11.2896MHz clock for 44.1 KHz audio data.

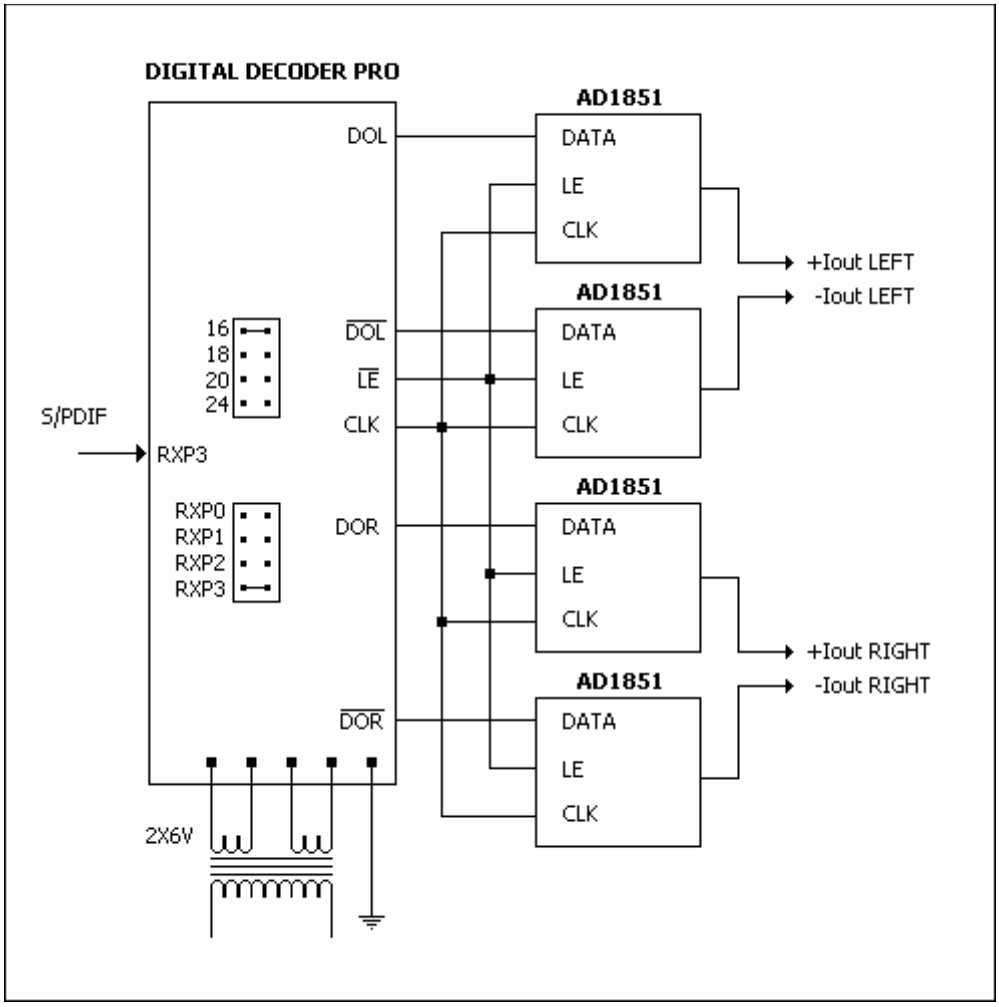


FIGURE 7 – Typical connection using four DAC for balanced current output.

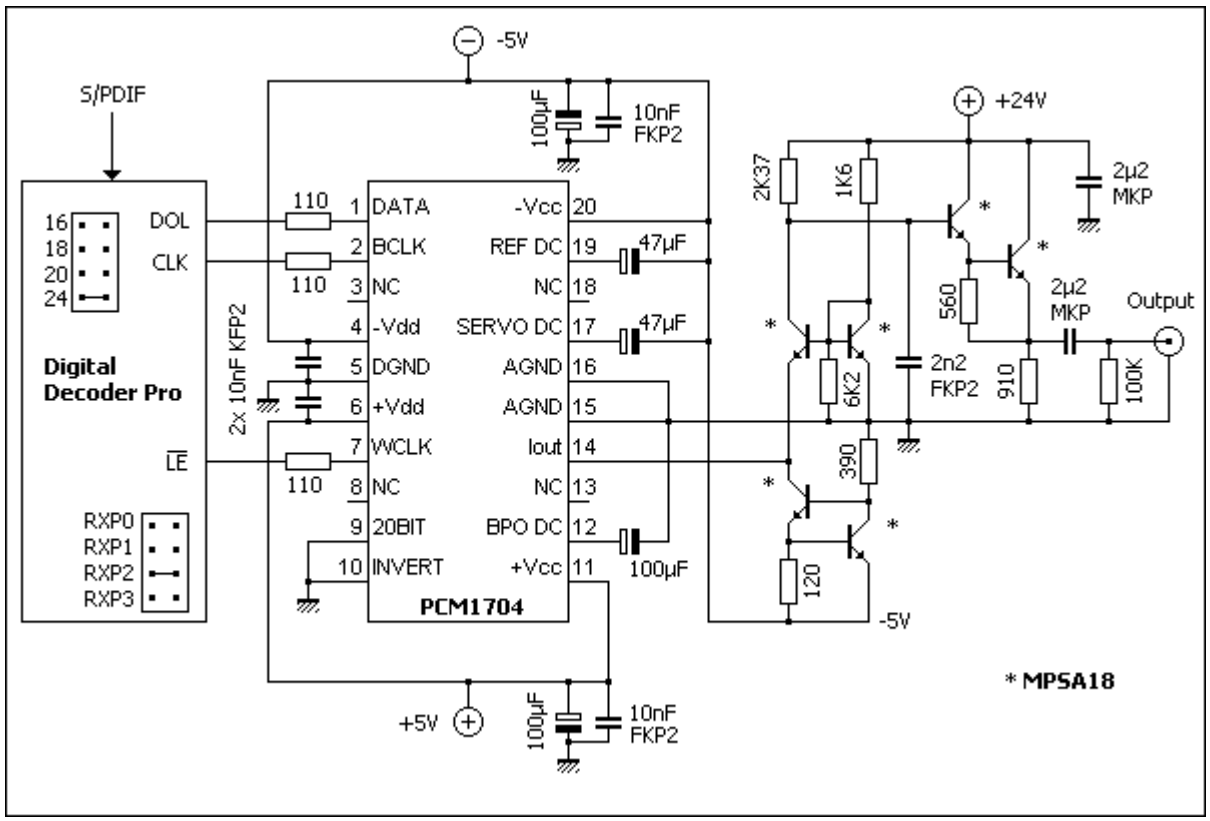


FIGURE 8 – Typical application circuit (one channel show) with 24 bit PCM1704 DAC, feedback free I/V converter and first order low pass filter (30.5 KHz).