Burr-Brown Products
from Texas Instruments

DF1706

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Stereo, 24-Bit, 192kHz
8x Oversampling Digital Interpolation Filter

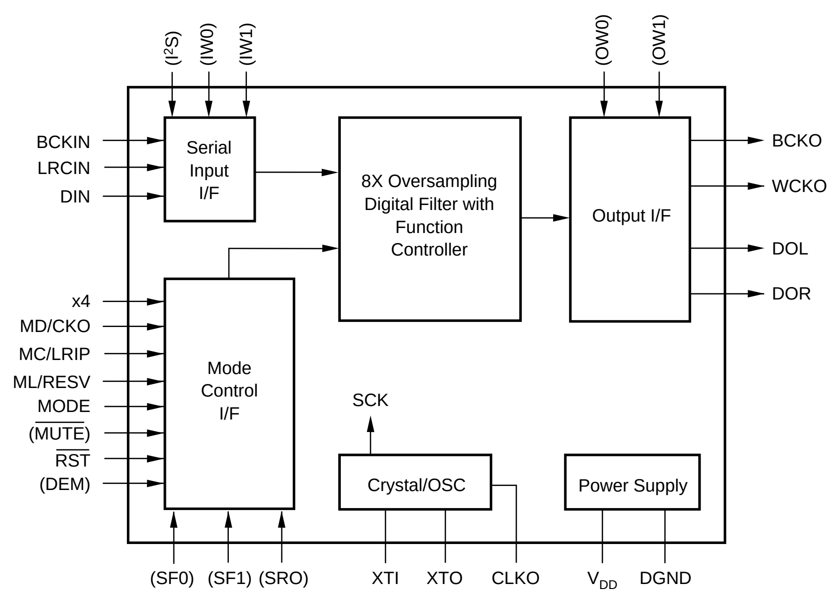
FEATURES

- **COMPANION DIGITAL FILTER FOR THE PCM1704 24-BIT AUDIO DAC**
- **HIGH PERFORMANCE FILTER:**
  Stopband Attenuation: –115dB
  Passband Ripple: ±0.00005dB
- **AUDIO INTERFACE:**
  Input Data Formats: Standard, Left-Justified, and I²S
  Input Word Length: 16, 20, or 24 Bits
  Output Word Length: 16, 18, 20, or 24 Bits
  Sampling Frequency: 32kHz to 192kHz
- **SYSTEM CLOCK: $128f_S$, $192f_S$, $256f_S$, $384f_S$, $512f_S$, $768f_S$**
- **ON-CHIP CRYSTAL OSCILLATOR**
- **PROGRAMMABLE FUNCTIONS:**
  Hardware or Software Control Modes
  Sharp or Slow Roll-Off Filter Response
  Soft Mute
  Digital De-Emphasis
  Independent Left/Right Digital Attenuation
- **+3.3V SINGLE-SUPPLY OPERATION**
- **SMALL SSOP-28 PACKAGE**

DESCRIPTION

The DF1706 is a high performance, stereo, 8X oversampling digital interpolation filter designed for high-end consumer and professional audio applications. The DF1706 supports 24-bit, 192kHz operation and features user-programmable functions, including selectable filter response, de-emphasis, attenuation, and input/output data formats.

The DF1706 is the ideal companion for Texas Instruments's PCM1704 24-bit audio Digital-to-Analog (D/A) converter. This combination allows for the construction of very high-performance audio systems and components.



TEXAS INSTRUMENTS

SBAS182
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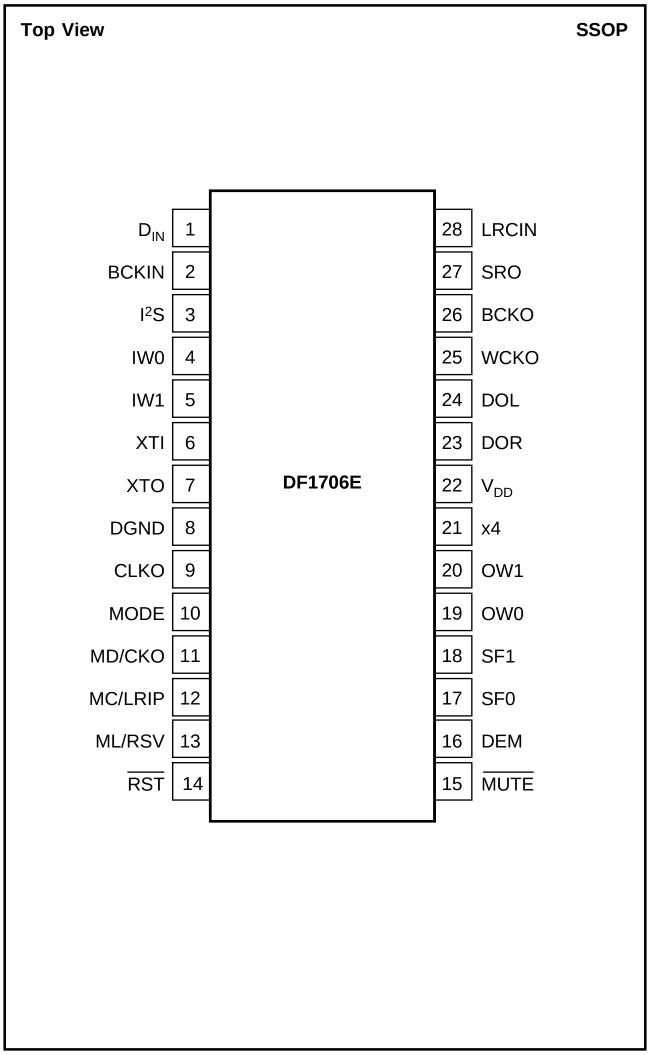
SPECIFICATIONS

All specifications at T_A = +25°C, V_{DD} = 3.3V, f_S = 44.1kHz, system clock = 256f_S/384f_S, 16-bit data, unless otherwise noted.

PARAMETER		CONDITIONS	DF1706E MIN	DF1706E TYP	DF1706E MAX	UNITS
RESOLUTION				24		Bits
INPUT DATA FORMAT						
Audio Data Interface Format				Standard, Left-Justified, I^2S		
Audio Data Bit Length				16, 20, 24 Selectable		
Audio Data Format				MSB First, Binary Two's Complement		
Sampling Frequency	f_S		32		192	kHz
System Clock Frequency(1)				128/192/256/384/512/768		f_S
OUTPUT DATA FORMAT						
Audio Data Interface Format				Right-Justified		
Audio Data Bit Length				16, 20, 24 Selectable		
Audio Data Format				MSB First, Binary Two's Complement		
DIGITAL INPUT/OUTPUT				CMOS Compatible		
Input Logic Level:	V_{IH}		0.7V_{DD}			V
	V_{IL}				0.3V_{DD}	V
Output Logic Level:	V_{OH}	I_{OH} = 2mA	2.4			V
	V_{OL}	I_{OL} = 4mA			1.0	V
CLKO AC CHARACTERISTICS(2)						
Rise Time	t_R	20% to 80% V_{DD}, 20pF		4		ns
Fall Time	t_F	80% to 20% V_{DD}, 20pF		3		ns
Duty Cycle(2)		20pF Load		50		%
DIGITAL FILTER PERFORMANCE						
Filter Characteristics 1 (Sharp Roll-Off)						
Passband		±0.00005dB			0.454	f_S
		–3dB			0.493	f_S
Stopband			0.546			f_S
Passband Ripple					±0.00005	dB
Stopband Attenuation		Stopband = 0.546f_S	–115			dB
Filter Characteristics 2 (Slow Roll-Off)						
Passband Ripple		±0.0001dB			0.254	f_S
		–3dB			0.460	f_S
Stopband			0.732			f_S
Passband Ripple					±0.0001	dB
Stopband Attenuation		Stopband = 0.748f_S	–100			dB
Delay Time				45.125/f_S		sec
De-Emphasis Error					±0.004	dB
POWER-SUPPLY REQUIREMENTS						
Voltage Range		V_{DD}	3.0	3.3	3.6	VDC
Supply Current	I_{DD}	V_{DD} = 3.3V		30	45	mA
Power Dissipation		V_{DD} = 3.3V		99	149	mW
TEMPERATURE RANGE						
Operation			–25		+85	°C
Storage			–55		+125	°C
Thermal Resistance, θ_{JA}		SSOP-28		100		°C

NOTES: (1) Refer to Table I. (2) Crystal resonator used.

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	D_{IN}	IN	Serial Audio Data Input(1)
2	BCKIN	IN	Bit Clock Input for Serial Audio Data(1)
3	I^2S	IN	Input Audio Data Format Select(2, 4)
4	IW0	IN	Input Audio Data Word Select(2, 4)
5	IW1	IN	Input Audio Data Word Select(2, 4)
6	XTI	IN	Oscillator Input/External Clock Input
7	XTO	OUT	Oscillator Output
8	DGND	—	Digital Ground
9	CLKO	OUT	Buffered System Clock Output
10	MODE	IN	Mode Control Select (HIGH: Software Mode, LOW: Hardware Mode)(3)
11	MD/CKO	IN	Mode Control, Data/Half External Clock Frequency Select(3, 5)
12	MC/LRIP	IN	Mode Control, Clock/Polarity of LRCIN Select(3, 5)
13	ML/RESV	IN	Mode Control, Latch Clock/Reserve(3, 5)
14	$\overline{RST}$	IN	Reset, Active LOW. When this pin is LOW the DF and modulators are held in reset.(3)
15	$\overline{MUTE}$	IN	Mute Control, Active LOW(4)
16	DEM	IN	De-Emphasis Control(2, 4)
17	SF0	IN	Sampling Rate Select for De-emphasis(2, 4)
18	SF1	IN	Sampling Rate Select for De-emphasis(2, 4)
19	OW0	IN	Output Audio Data Word Select(2, 4)
20	OW1	IN	Output Audio Data Word Select(2, 4)
21	x4	IN	Oversampling Ratio Control. When this pin is set HIGH, the ratio is 4 times.
22	V_{DD}	—	Digital Power, +3.3V
23	DOR	OUT	R-Channel, Serial Audio Data Output
24	DOL	OUT	L-Channel, Serial Audio Data Output
25	WCKO	OUT	Word Clock Output for Serial Audio Data Output
26	BCKO	OUT	Bit Clock Output for Serial Audio Data Output
27	SRO	IN	Filter Response Select (2, 4)
28	LRCIN	IN	L/R Clock Input (f_S)(1)

NOTES: (1) Pins 1, 2, 28—Schmitt-Trigger input without pull-up and -down resistor. (2) Pins 3-5, 16-21, 27—Schmitt-Trigger input without pull-up and -down resistor. (3) Pins 10-15—Schmitt-Trigger input without pull-up and -down resistor. (4) Pins 3-5, 15-20, 27—these pins are invalid when MODE (pin 10) is HIGH. (5) Pins 11-13—these pins have different functions corresponding to MODE (pin 10) HIGH/LOW.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +4.0V
Digital Input Voltage .... –0.2V to 4.5V
Input Current (any pins except supplies) .... ±10mA
Operating Temperature Range .... –25°C to +85°C
Ambient Storage Temperature .... –40°C to +125°C
Junction Temperature .... +150°C
Lead Temperature (soldering, 5s) .... +260°C
Package Temperature (IR reflow, Peak, 10s) .... +235°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

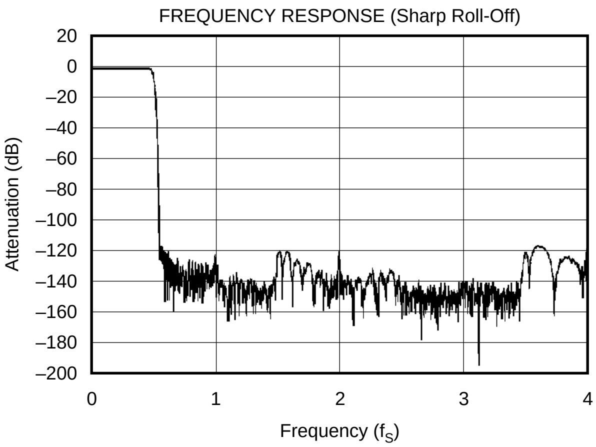
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
DF1706E	SSOP-28	324	–25°C to +85°C	DF1706E	DF1706E	Rails
"	"	"	"	"	DF1706E/2K	Tape and Reel

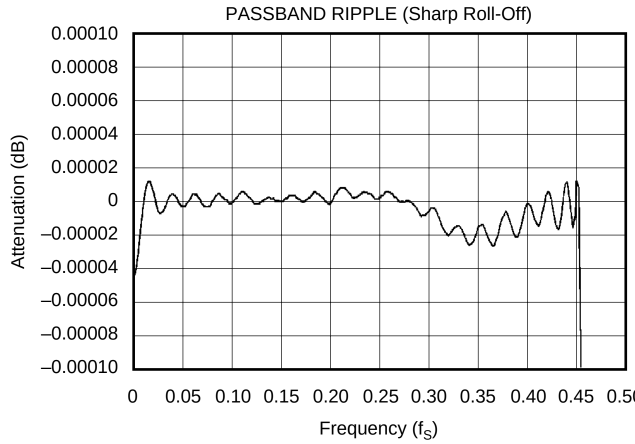
NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of “DF1706E/2K” will get a single 2000-piece Tape and Reel.

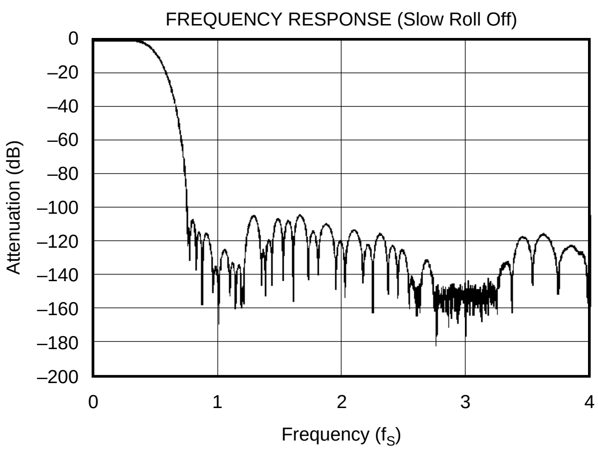
TYPICAL PERFORMANCE CURVES

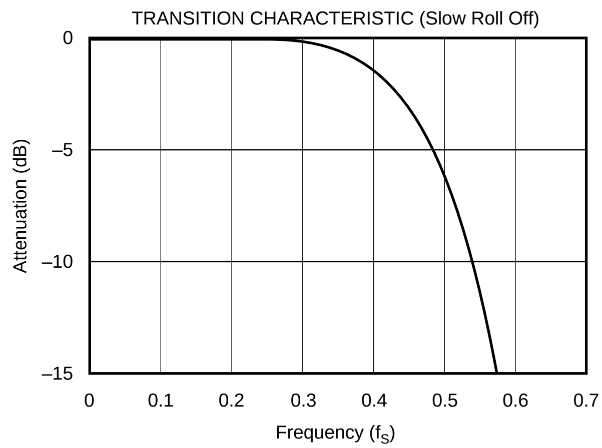
At T_A = +25°C, V_{DD} = ±3.3V, f_S = 44.1kHz, System Clock = $256f_S/384f_S$, 16-bit data, unless otherwise noted.

DIGITAL FILTER (DE-EMPHASIS OFF, f_S = 44.1kHz)

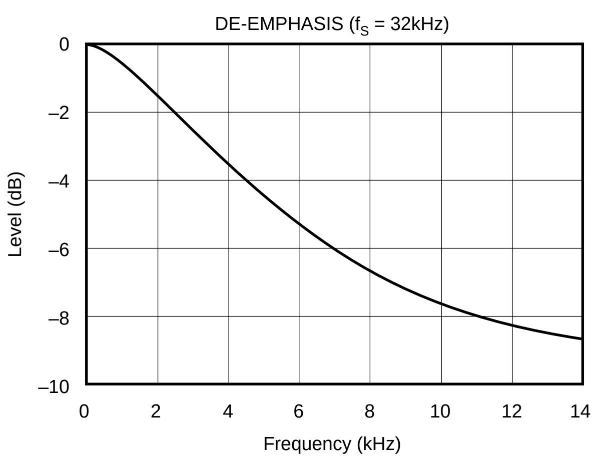


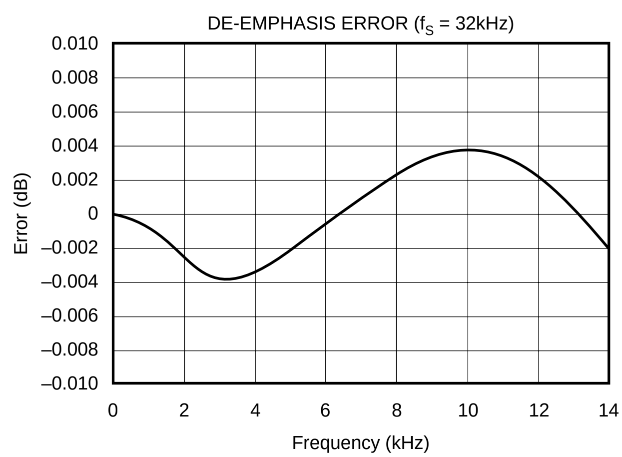






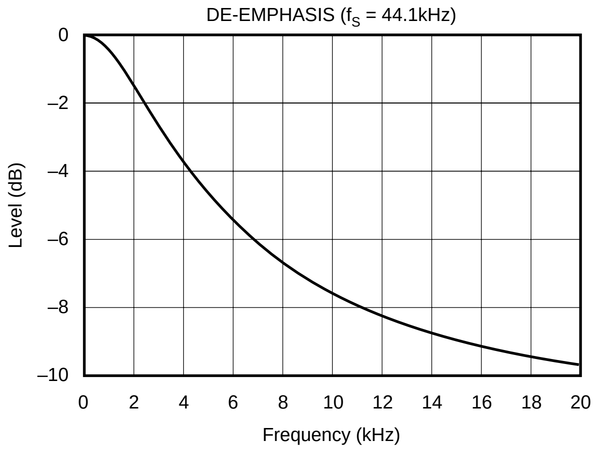
DE-EMPHASIS AND DE-EMPHASIS ERROR

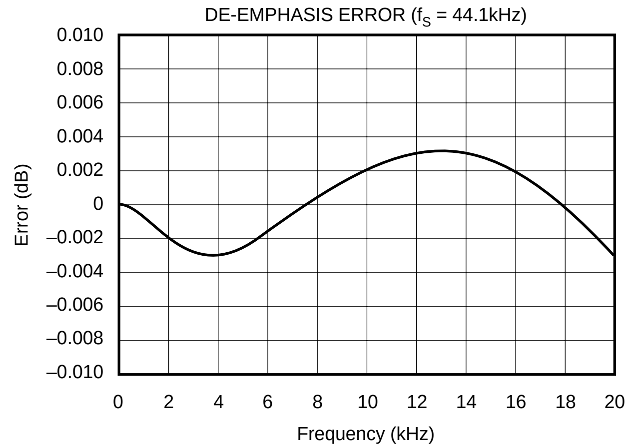


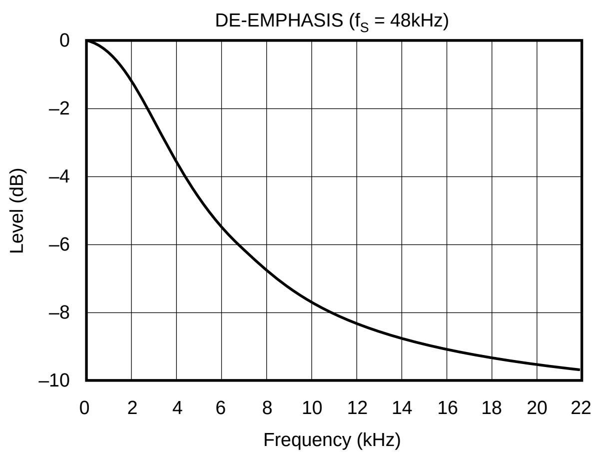


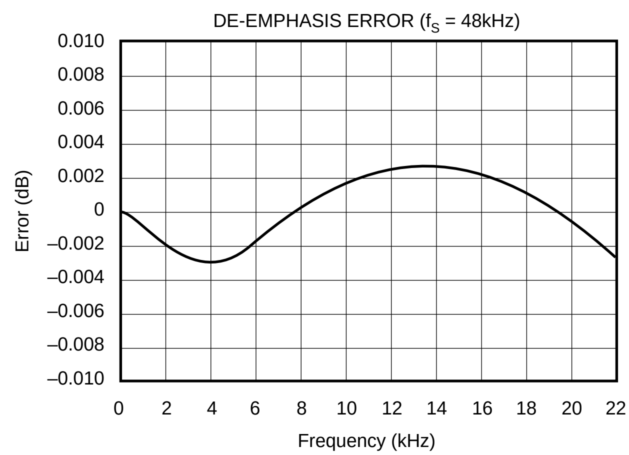
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_{DD} = ±3.3V, f_S = 44.1kHz, System Clock = $256f_S/384f_S$, 16-bit data, unless otherwise noted.









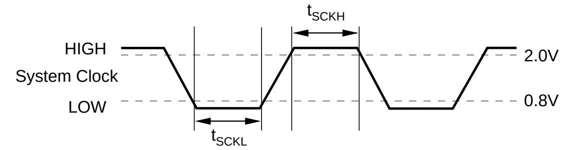
SYSTEM CLOCK REQUIREMENTS

The system clock of the DF1706 can be supplied by either an external clock signal at XTI (pin 6), or by the on-chip crystal oscillator. The system clock rate must run at $128f_S$, $192f_S$, $256f_S$, $384f_S$, $512f_S$, or $768f_S$, where f_S is the audio sampling rate. When a $128f_S$ or $192f_S$ system clock is applied to DF1706, the Over-Sampling Ratio (OSR) of the DF1706's digital filter should be four times instead of eight times. The OSR can be selected by the x4 pin (pin 21) in hardware mode or x4 bit on MODE 2 register in software mode.

It should be noted that a $768f_S$ system clock cannot be used when f_S is larger than 48kHz. Both $128f_S$ and $192f_S$ system clock can be used when f_S is larger than 96kHz. In addition, the on-chip crystal oscillator is limited to a maximum frequency of 24.0MHz. Table I shows the typical system clock frequencies for selected sample rates.

The DF1706 includes a system clock detection circuit that determines the system clock rate in use. The circuit compares the system clock input (XTI) frequency with the LRCIN input rate to determine the system clock multiplier. Ideally, LRCIN and BCKIN should be derived from the system clock to ensure proper synchronization. If the phase difference between the system clock and LRCIN is larger than ±4 bit clock (BCKIN) periods, the synchronization of the system and LRCIN clocks will be performed automatically by the DF1706.

Timing requirements for the system clock input are shown in Figure 1.



SYMBOL	PARAMETERS	MIN	MAX	UNITS
t_{SCKH}	System Clock Pulse Width HIGH	12		ns(1)
t_{SCKL}	System Clock Pulse Width LOW	12		ns(1)

NOTE: (1) For f_S = 96kHz and SCK = $256f_S$, t_{SCKIH} = 14ns (min)
t_{SCKIL} = 14ns (min)
For $f_S \neq$ 96kHz and SCK = $256f_S$, t_{SCKIH} = 20ns (min)
t_{SCKIL} = 20ns (min)

FIGURE 1. System Clock Timing.

RESET

The DF1706 has both an internal power-on reset circuit and a reset pin, $\overline{RST}$ (pin 14), for providing an external reset signal. The internal power-on reset is performed automatically when power is applied to the DF1706, as shown in Figure 2. The $\overline{RST}$ pin can be used to synchronize the DF1706 with a system reset signal, as shown in Figure 3.

During the power-on reset period (1024 system clocks), the outputs of BCKO, DOL, and DOR are forced LOW and the output of WCKO is forced HIGH. For an external forced reset, the outputs of BCKO, DOL, and DOR are forced LOW and the output of WCKO is forced HIGH during the initialization period (1024 system clocks), which occurs after the LOW-to-HIGH transition of the $\overline{RST}$ pin (see Figure 3).

SAMPLING RATE FREQUENCY (f_S)$256f_S$	SYSTEM CLOCK FREQUENCY (MHz)					
	$128f_S$	$192f_S$	$256f_S$	$384f_S$	$512f_S$	$768f_S$
32kHz	N/A	N/A	8.192	12.288	16.384	24.576(1)
44.1kHz	N/A	N/A	11.2896	16.934	22.5792	33.8688(1)
48kHz	N/A	N/A	12.288	18.432	24.576(1)	36.864(1)
88.2kHz	N/A	N/A	22.5792(1)	33.8688(1)	N/A	N/A
96kHz	N/A	N/A	24.576	36.864(1)	N/A	N/A
176.4kHz	22.5792(2)	33.8688(1)(2)	N/A	N/A	N/A	N/A
192kHz	24.576(1)(2)	36.864(1)(2)	N/A	N/A	N/A	N/A

NOTES: (1) Crystal oscillator frequency using internal oscillator is not covered at frequency larger than 24.0MHz. (2) x4 (pin 21) should be set to HIGH.

TABLE I. Typical System Clock Frequencies.

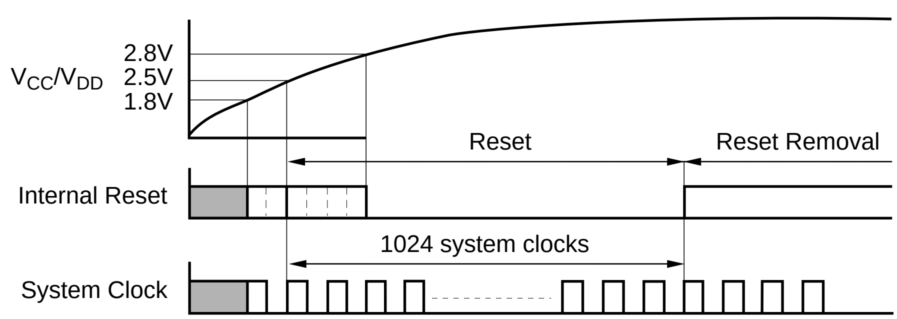


FIGURE 2. Internal Power-On Reset Timing.

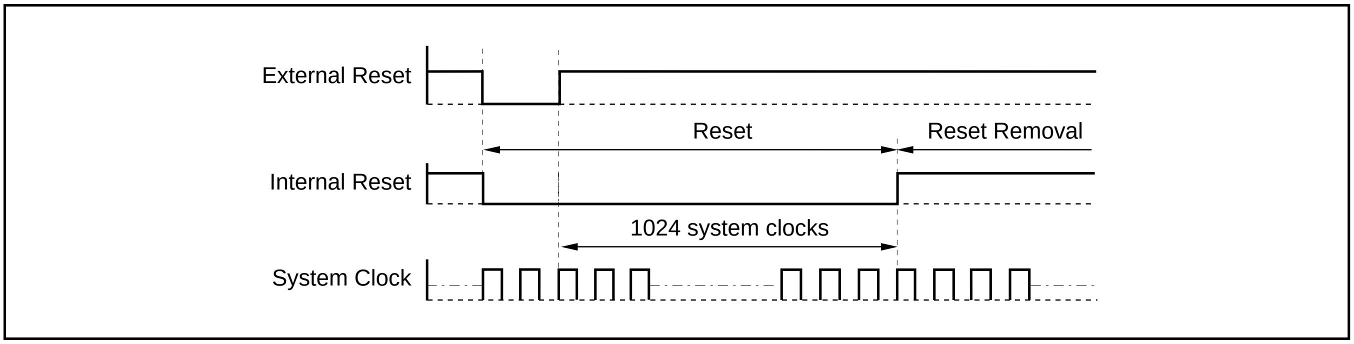


FIGURE 3. External Forces Reset Timing.

AUDIO INPUT INTERFACE

The audio input interface is comprised of BCKIN (pin 2), LRCIN (pin 28), and DIN (pin 1). BCKIN is the input bit clock, which is used to clock data applied at D_{IN} into the DF1706's input serial interface. Input data at D_{IN} is clocked into the DF1706 on the rising edge of BCKIN. The left/right clock, LRCIN, is used as a word latch for the audio input data. BCKIN can run at $32f_S$, $48f_S$, or $64f_S$, where f_S is the audio sample frequency. LRCIN is run at the f_S rate. Figures 4 (a) through (c) show the input data formats, which are selected by hardware or software controls.

See Figure 5 for the audio input interface timing requirements.

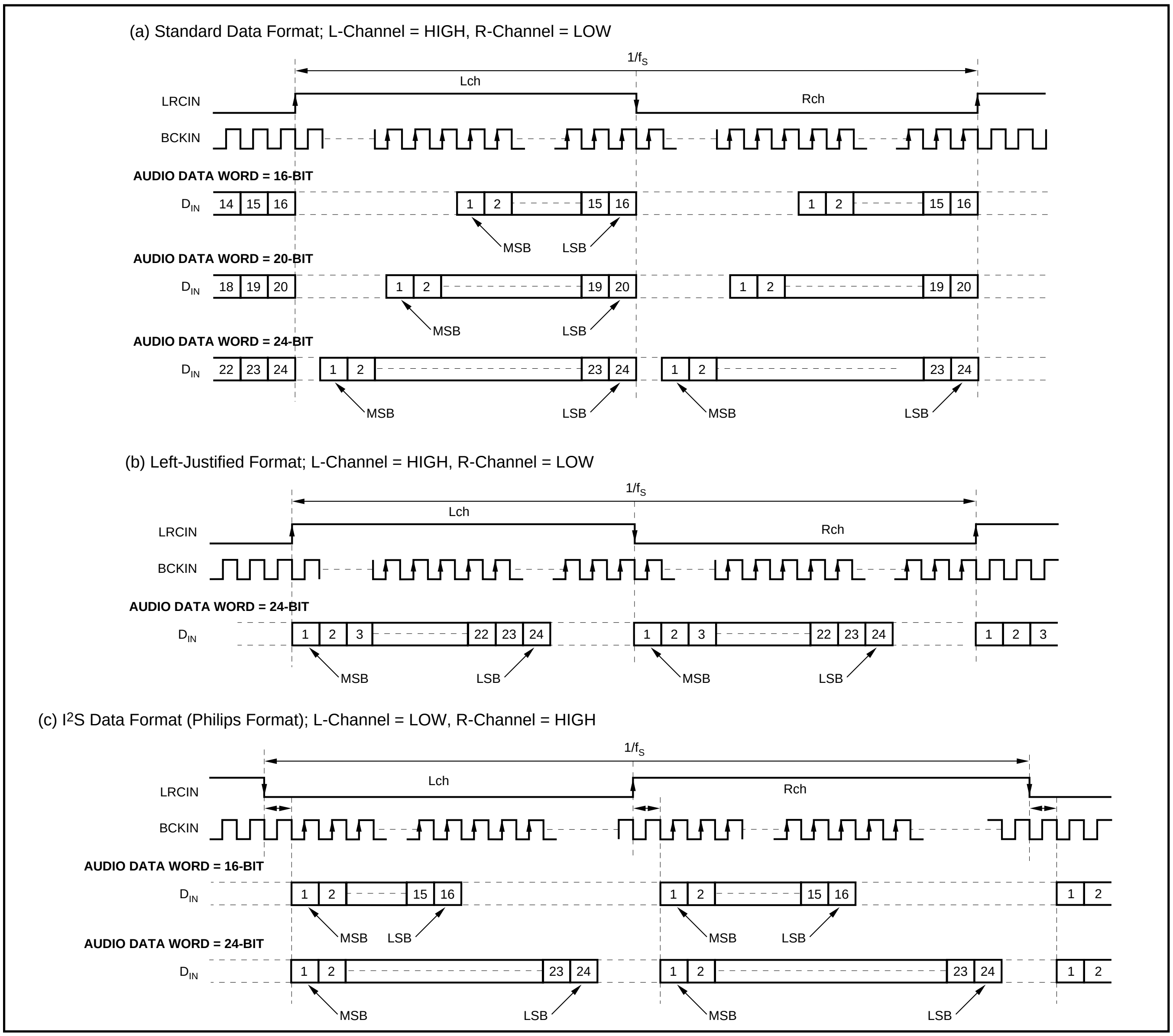


FIGURE 4. Audio Data Input Formats.

AUDIO OUTPUT INTERFACE

The audio output interface includes BCKO (pin 26), WCKO (pin 25), DOL (pin 24), and DOR (pin 23).

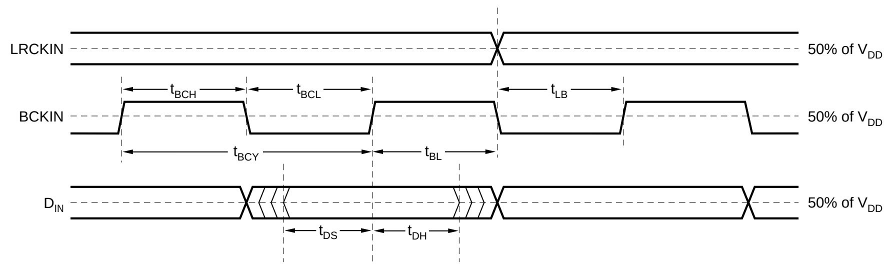
BCKO is the output bit clock and is used to clock data into an audio D/A converter, such as the PCM1704. DOL and DOR are the left and right audio data outputs. WCKO is the output word clock and is used to latch audio data words into an audio D/A converter.

WCKO runs at a fixed rate of $8f_S$ (8x oversampling) for all system clock rates.

BCKO is fixed at $256f_S$ for system clock rates of $256f_S$ or $512f_S$.

BCKO is fixed at $192f_S$ for system clock rates of $384f_S$ or $768f_S$.

The output data format used by the DF1706 for DOL and DOR is Binary Two's Complement, MSB-first, right-justified audio data. Figures 6(a), (b), (c), and (d) show the output data formats for the DF1706. See Figure 7 the audio output timing.



BCKIN Pulse Cycle Time	t_{BCY}	82ns (min)
BCKIN Pulse Width LOW	t_{BCL}	35ns (min)
BCKIN Pulse Width HIGH	t_{BCH}	35ns (min)
BCKIN Rising Edge to LRCIN Edge	t_{BL}	10ns (min)
LRCIN Edge to BCK Rising Edge	t_{LB}	10ns (min)
D_{IN} Set-up Time	t_{DS}	10ns (min)
D_{IN} Hold Time	t_{DH}	10ns (min)

FIGURE 5. Audio Input Interface Timing.

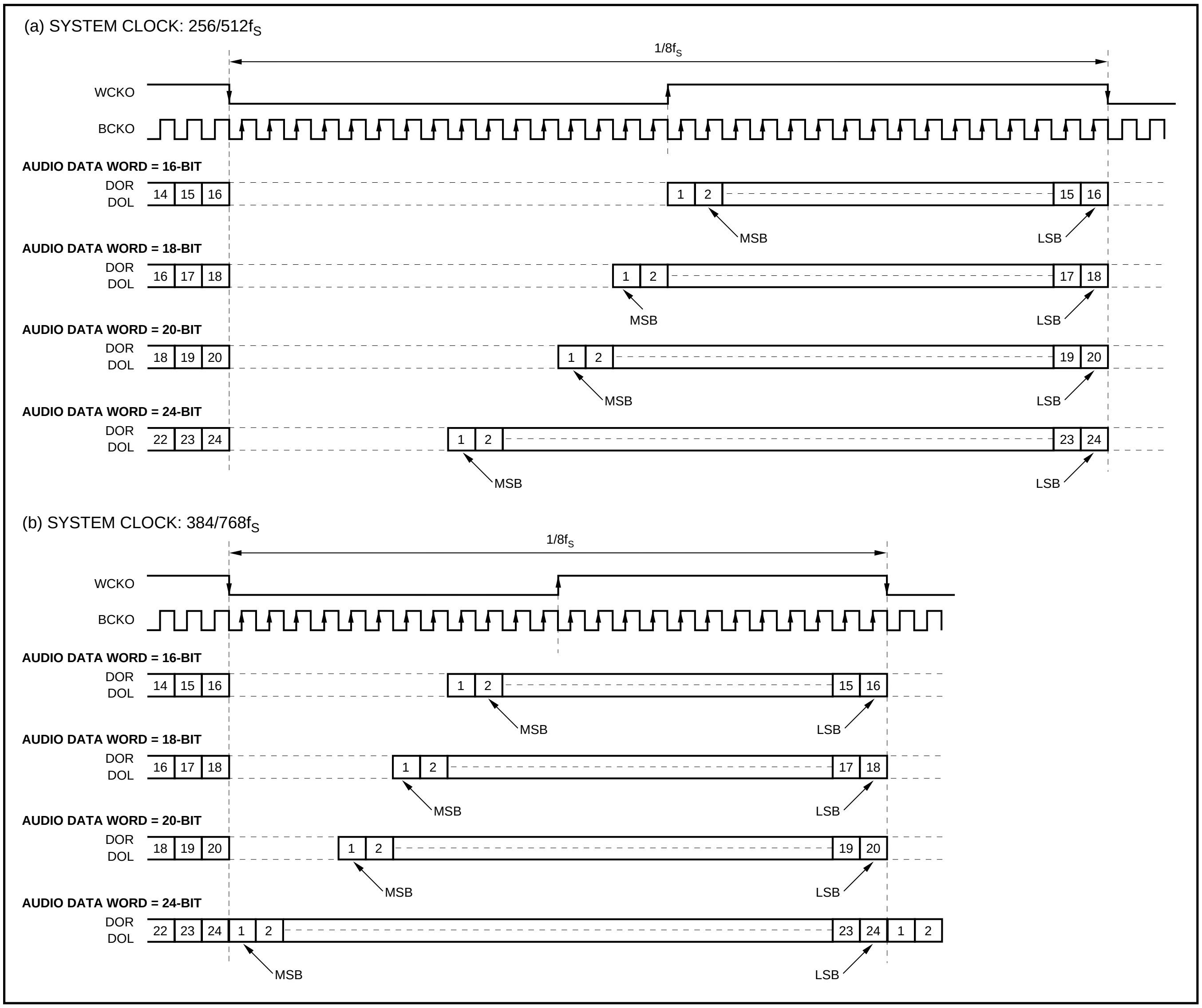
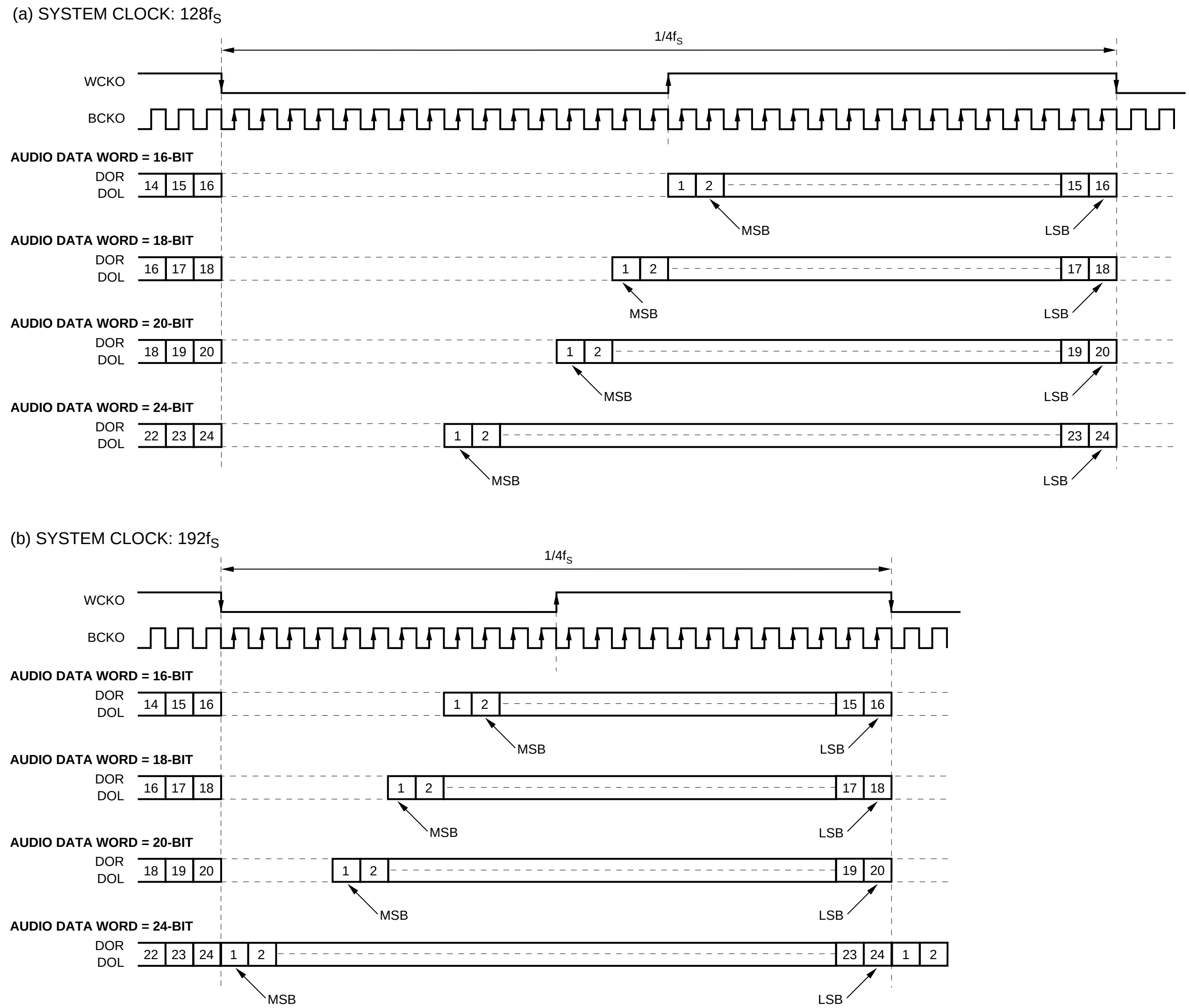


FIGURE 6. Audio Output Data Format.



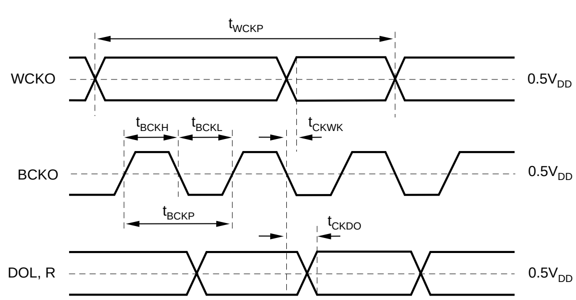
(Cont.) FIGURE 6. Audio Output Data Format.

MODE CONTROL

The DF1706 may be configured using either software or hardware control. The selection is made using the MODE input (pin 10). See Table II for MODE selection.

MODE SETTING	MODE CONTROL SELECTION
MODE = H MODE = L	Software Mode Hardware Mode

TABLE II. MODE Selection.



PARAMETERS		SYMBOL	MIN	TYP	MAX	UNITS
BCKO Period		t_{BCKP}	1/96f_S, 1/128f_S, 1/192f_S, 1/256f_S,			
BCKO Pulse Width HIGH/LOW	(f_S = 192kHz, 192f_S)	t_{BCKH}/t_{BCKL}	10		20	ns
	(f_S = 192kHz, 128f_S)		14		30	ns
	(other f_S, 256/384/512/768f_S)		20		100	ns
Delay Time BCKO Falling Edge to WCKO Valid		t_{CKWK}	–5		5	ns
WCKO Period		t_{WCKP}		1/4f_S, 1/8f_S		
Delay Time BCKO Falling Edge to DOL, R Valid		t_{CKDO}	–5		5	ns
Rising Time of All Signals		t_R	7			ns
Falling Time of All Signals		t_F	7			ns

NOTE: (1) Rising and falling time is measured from 10% to 90% of IN/OUT signal swing. (2) Load capacitance of all signals are 20pF.

FIGURE 7. Audio Data Output Timing.

Programmable Functions

The DF1706 includes a number of programmable features, with most being accessible from either Hardware or Software mode. Table III summarizes the user-programmable functions for both modes of operation.

FUNCTION	SOFTWARE (MODE = H)	HARDWARE (MODE = L)	RESET DEFAULT (Software Mode)
Input Data Format Selection	O	O	Standard Format
Input Word Length Selection	O	O	16 Bits
Output Word Length Selection	O	O	16 Bits
LRCIN Polarity Selection	O	O	Left/Right = High/Low
Digital De-Emphasis	O	O	OFF
Over Sample Ratio Control	O	O	8x
Soft Mute	O	O	OFF
Digital Attenuation	O	X	0dB, Independent L/R
Sample Rate for De-Emphasis Function	O	O	44.1 kHz
Filter Roll-Off Selection	O	O	Sharp Roll-Off Selected
CLKO Output-Frequency Selection	O	O	Same As XTI Input
Legend: O = User Programmable, X = Not Available.			

TABLE III. User-Programmable Functions for Software and Hardware Mode.

Hardware Mode Controls

With MODE = L, the DF1706 may be configured by utilizing several user-programmable pins. The following is a brief summary of the pin functions. Table IV provides more details on setting the hardware mode controls.

Pins I^2S, IW0, and IW1 are used to select the audio data input format and word length.

Pins OW0 and OW1 are used to select the output data word length.

The DEM pin is used to enable and disable the digital de-emphasis function. De-emphasis is only available for 32kHz, 44.1kHz, and 48kHz sample rates.

Pins SF0 and SF1 are used to select the sample rate for the de-emphasis function.

The SRO pin is used to select the digital filter response, either sharp or slow roll-off. Generally, sharp roll-off filter is used.

The MUTE pin is used to enable or disable the soft mute function.

The CKO pin is used to select the clock frequency seen at the CLKO pin, either XTI or XTI ÷ 2.

The LRIP pin is used to select the polarity used for the audio input left/right clock, LRCIN.

The x4 pin is used to control the over sampling ratio of the internal digital filter, either a 8x or 4x. For instance, when fs is 192kHz or 176.4kHz, the over sampling ratio should be 4x.

PIN NAME	PIN NUMBER	DESCRIPTION
RSV	13	Reserved, Not Used
LRIP	12	LRCIN Polarity LRIP = H: LRCIN= H = Left Channel, LRCIN= L = Right Channel LRIP = L: LRCIN= L = Left Channel, LRCIN = H = Right Channel
CKO	11	CLKO Output Frequency CKO = H: CLKO Frequency = XTI/2 CKO = L: CLKO Frequency = XTI
MUTE	15	Soft Mute Control: H = Mute Off, L = Mute On
I^2S IW0 IW1	3 4 5	Input Data Format Controls **I^2S IW1 IW0 INPUT FORMAT** L L L 16-Bit, Standard, MSB-First, Right-Justified L L H 20-Bit, Standard, MSB-First, Right-Justified L H L 24-Bit, Standard, MSB-First, Right-Justified L H H 24-Bit, MSB-First, Left-Justified H L L 16-Bit, I^2S H L H 24-Bit, I^2S
SRO	27	Digital Filter Roll-Off: H = Slow, L = Sharp
OW0 OW1	19 20	Output Data Word Length Controls **OW1 OW0 OUTPUT FORMAT** L L 16-Bit, MSB-First L H 18-Bit, MSB-First H L 20-Bit, MSB-First H H 24-Bit, MSB-First
SF0 SF1	17 18	Sample Rate Selection for the Digital De-Emphasis Control **SF1 SF0 SAMPLING RATE** L L 44.1kHz L H Reserved, Not Used H L 48kHz H H 32kHz
DEM	16	Digital De-Emphasis: H = On, L = Off
x4	21	Oversampling Rate Control: H = $4f_S$, L = $8f_S$

TABLE IV. Hardware Mode Controls.

Finally, the RESV pin is not used by the current DF1706 design, but is reserved for future use.

Software Mode Controls

With MODE = H, the DF1706 may be configured by programming four internal registers in software mode. ML (pin 13), MC (pin 12), and MD (pin 11) make up the 3-wire software control port, and may be controlled using DSP or microcontroller general purpose I/O pins, or a serial port. Table V provides an overview of the internal registers, labeled MODE0 through MODE3 (see Table V).

See Figures 8 through 10 for more details regarding the control port data format and timing requirements. The data format for the control port is 16-bit, MSB-first, with Bit B15 being the MSB.

Register Addressing

A[1:0], bits B10 and B9 of the 16-bit control data word, are used to indicate the register address to be written to by the current control port write cycle. See Table VI for how to address the internal registers using bits A[1:0] of registers MODE0 through MODE3.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
MODE0	res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
MODE1	res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
MODE2	res	res	res	res	res	A1	A0	res	res	OW1	OW0	IW1	IW0	x4	DEM	MUT
MODE3	res	res	res	res	res	A1	A0	res	SF1	SF0	CKO	res	SRO	ATC	LRP	I^2S

FIGURE 8. Internal Mode Control Registers.

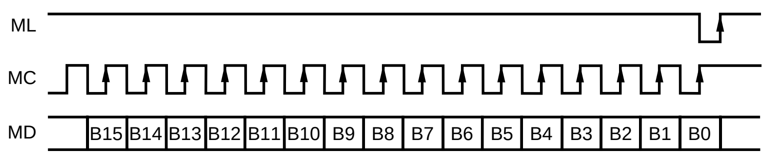
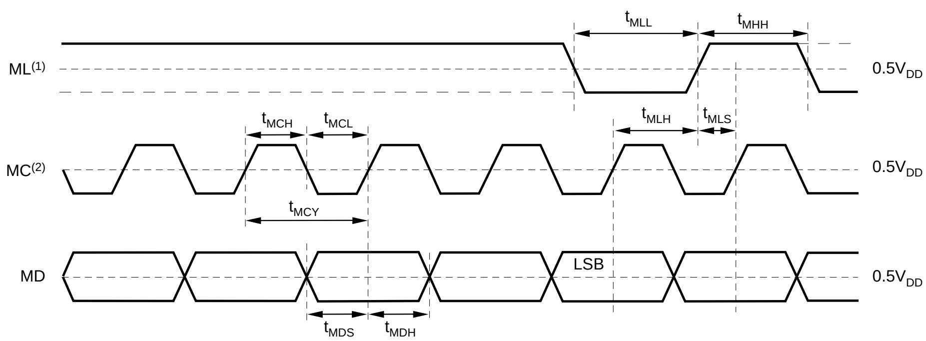


FIGURE 9. Software Interface Format.



MC Pulse Cycle Time	t_{MCY}	100ns (min)
MC Pulse Width LOW	t_{MCL}	40ns (min)
MC Pulse Width HIGH	t_{MCH}	40ns (min)
MD Hold Time	t_{MDH}	10ns (min)
MD Set-Up Time	t_{MDS}	10ns (min)
ML LOW Level Time	t_{MLL}	40ns
ML HIGH Level Time	t_{MHH}	40ns
ML Hold Time(1)	t_{MLH}	20ns (min)
ML Set-Up Time(2)	t_{MLS}	20ns (min)

NOTES: (1) ML rising edge to the next MC rising edge.
(2) MC rising edge for LSB to ML rising edge.

FIGURE 10. Software Interface Timing Requirements.

REGISTER NAME	BIT NAME	DESCRIPTION
MODE0	AL[7:0]	Attenuation Data for the Left Channel
	LDL	Attenuation Load Control for the Left Channel
	A[1:0]	Register Address
	res	Reserved
MODE1	AR[7:0]	Attenuation Data for the Right Channel
	LDL	Attenuation Load Control for the Right Channel
	A[1:0]	Register Address
	res	Reserved
MODE2	MUT	Soft Mute Control
	DEM	Digital De-Emphasis Control
	x4	Oversampling Rate Control
	IW[1:0]	Input Data Format and Word Length
	OW[1:0]	Output Data Word Length
	A[1:0]	Register Address
	res	Reserved
MODE3	I^2S	Input Data Format (I^2S or Standard/Left-Justified)
	LRP	LRCIN Polarity
	ATC	Attenuator Control, Dependent or Independent
	SRO	Digital Filter Roll-Off Selection (sharp or slow)
	CKO	CLKO Frequency Selection (XTI or XTI ÷ 2)
	SF[1:0]	Sample Rate Selection for De-Emphasis Function
	A[1:0]	Register Address
	res	Reserved

NOTE: All reserved bits should be programmed to 0.

TABLE V. Internal Register Mapping.

A1	A0	REGISTER SELECTED
0	0	MODE0
0	1	MODE1
1	0	MODE2
1	1	MODE3

TABLE VI. Internal Register Addressing.

MODE0 Register

The MODE0 register is used to set the attenuation data for the left output channel, or DOL (pin 24).

When ATC = 1 (Bit B2 of Register MODE3 = 1), the left channel attenuation data AL[7:0] is used for both the left and right channel attenuators.

When ATC = 0, (Bit B2 of Register MODE3 = 0), left channel attenuation data is taken from AL[7:0] of register MODE0, and right channel attenuation data is taken from AR[7:0] of register MODE1.

AL[7:0] Left Channel Attenuator Data, where AL7 is the MSB and AL0 is the LSB.
Attenuation Level is given by:

ATTEN = 0.5 • (DATA – 255)dB

For DATA = FF_H, ATTEN = –0dB
For DATA = FE_H, ATTEN = –0.5dB
For DATA = 01_H, ATTEN = –127.5dB
For DATA = 00_H, ATTEN = infinity = Mute

LDL Left Channel Attenuation Data Load Control. This bit is used to simultaneously set attenuation levels of both the left and right channels.

When LDL = 1, the left channel output level is set by the data in AL[7:0]. The right channel output level is set by the data in AL[7:0], or the most recently programmed data in bits AR[7:0] of register MODE1.

When LDL = 0, the left channel output data remains at its previously programmed level.

MODE1 Register

The MODE1 register is used to set the attenuation data for the right output channel, or DOR (pin 23).

When ATC = 1 (Bit B2 of Register MODE3 = 1), the left channel attenuation data AL[7:0] of register MODE0 is used for both the left and right channel attenuators.

When ATC = 0, (Bit B2 of Register MODE3 = 0), left channel attenuation data is taken from AL[7:0] of register MODE0, and right channel attenuation data is taken from AR[7:0] of register MODE1.

AR[7:0] Right Channel Attenuator Data, where AR7 is the MSB and AR0 is the LSB. Attenuation Level is given by:

ATTEN = 0.5 • (DATA – 255)dB

For DATA = FF_H, ATTEN = –0dB
For DATA = FE_H, ATTEN = –0.5dB
For DATA = 01_H, ATTEN = –127.5dB
For DATA = 00_H, ATTEN = infinity = Mute

LDR Right Channel Attenuation Data Load Control. This bit is used to simultaneously set attenuation levels of both the left and right channels.

When LDR = 1, the right channel output level is set by the data in AR[7:0], or by the data in bits AL[7:0] of register MODE0. The left channel output level is set to the most recently programmed data in bits AL[7:0] of register MODE0.

When LDR = 0, the right channel output data remains at its previously programmed level.

MODE2 Register

The MODE2 register is used to program various functions:

MUT Soft Mute Function.

When MUT = 0, Soft Mute is ON for both left and right channels.
When MUT = 1, Soft Mute is OFF for both left and right channels.

DEM Digital De-Emphasis Function.

When DEM = 0, de-emphasis is OFF.
When DEM = 1, de-emphasis is ON.
x4 Oversampling Rate Selection
When x4 = 0, $8f_S$ Sampling Rate Operation
When x4 = 1, $4f_S$ Sampling Rate Operation

IW[1:0] Input Data Format and Word Length.

I^2S	IW1	IW0	Description
0	0	0	16-Bit Data, Standard Format (MSB-First, Right-Justified)
0	0	1	20-Bit Data, Standard Format
0	1	0	24-Bit Data, Standard Format
0	1	1	24-Bit Data, MSB-First, Left-Justified
1	0	0	16-Bit Data, I^2S Format
1	0	1	24-Bit Data, I^2S format
1	1	0	Reserved
1	1	1	Reserved

OW[1:0] Output Data Word Length.

OW1	OW0	Description
0	0	16-Bit Data, MSB-First
0	1	18-Bit Data, MSB-First
1	0	20-Bit Data, MSB-First
1	1	24-Bit Data, MSB-First

MODE3 Register

The MODE3 register is used to program various functions.

I^2S Input Data Format.

When I^2S = 0, standard or left-justified formats are enabled.

When I^2S = 1, the I^2S formats are enabled.

LRP LRCIN Polarity Selection.

When LRP = 0, left channel is HIGH and right channel is LOW.

When LRP = 1, left channel is LOW and right channel is HIGH.

ATC Attenuator Control.

This bit is used to determine whether the Left and Right channel attenuators operate with independent data, or use common data (the Left channel data in bits AL[7:0] of register MODE0).

When ATC = 0, the Left and Right channel attenuator data is independent.

When ATC = 1, the Left and Right channel attenuators use common data.

SRO Digital Filter Roll-Off Selection.

When SRO = 0, sharp roll-off is selected.
When SRO = 1, slow roll-off is selected.

CKO CLKO Output Frequency Selection.

When CKO = 0, the CLKO frequency is the same as the clock at the XTI input.
When CKO =1, the CLKO frequency is half of the XTI input clock frequency.

SF[1:0] Sampling Frequency Selection for the De-Emphasis Function.

SF1	SF0	Description
0	0	44.1 kHz
0	1	Reserved
1	0	48 kHz
1	1	32 kHz

APPLICATIONS INFORMATION

PCB LAYOUT GUIDELINES

In order to obtain the specified performance from the DF1706 and its associated D/A converters, proper printed circuit board layout is essential. Figure 11 shows two approaches for obtaining the best audio performance.

Figure 11(a) shows a standard, mixed signal layout scheme. The board is divided into digital and analog sections, each with its own ground. The ground areas should be put on a split-plane, separate from the routing and power layers. The DF1706 and all digital circuitry should be placed over the digital section, while the audio D/A converter(s) and analog circuitry should be located over the analog section of the board. A common connection between the digital and analog grounds is required and is done at a single point as shown.

For Figure 11(a), digital signals should be routed from the DF1706 to the audio D/A converter(s) using short, direct connections to reduce the amount of radiated high-frequency energy. If necessary, series resistors may be placed in the clock and data signal paths to reduce or eliminate any overshoot or undershoot present on these signals. A value of 50Ω to 100Ω is recommended as a starting point, but the designer should experiment with the resistor values in order to obtain the best results.

Figure 11(b) shows an improved method for high-performance, mixed signal board layout. This method adds digital isolation between the DF1706 and the audio D/A converter(s), and provides complete isolation between the digital and analog sections of the board. The ISO150 dual digital coupler provides excellent isolation, and operates at speeds up to 80Mbps.

POWER SUPPLIES AND BYPASSING

The DF1706 requires a single +5V power supply for operation. The power supply should be bypassed by a 10μF and 0.1μF parallel capacitor combination. The capacitors should be placed as close as possible to V_{DD} (pin 22). Aluminum electrolytics or tantalum capacitors can be used for the 10μF value, while ceramics may be used for the 0.1μF value.

BASIC CIRCUIT CONNECTIONS

See Figures 12 and 13 for basic circuit connections of the DF1706. Figure 12 shows connections for Hardware mode controls, while Figure 13 shows connections for Software mode controls. Notice the placement of C_1 and C_2 in both figures, as they are physically close to the DF1706.

TYPICAL APPLICATIONS

The DF1706 will typically be used in high performance audio equipment, in conjunction with high performance audio D/A converters. Figure 14 shows a typical application circuit example, employing the DF1706, a digital audio receiver, and two PCM1704 24-bit, 192kHz audio D/A converter(s).

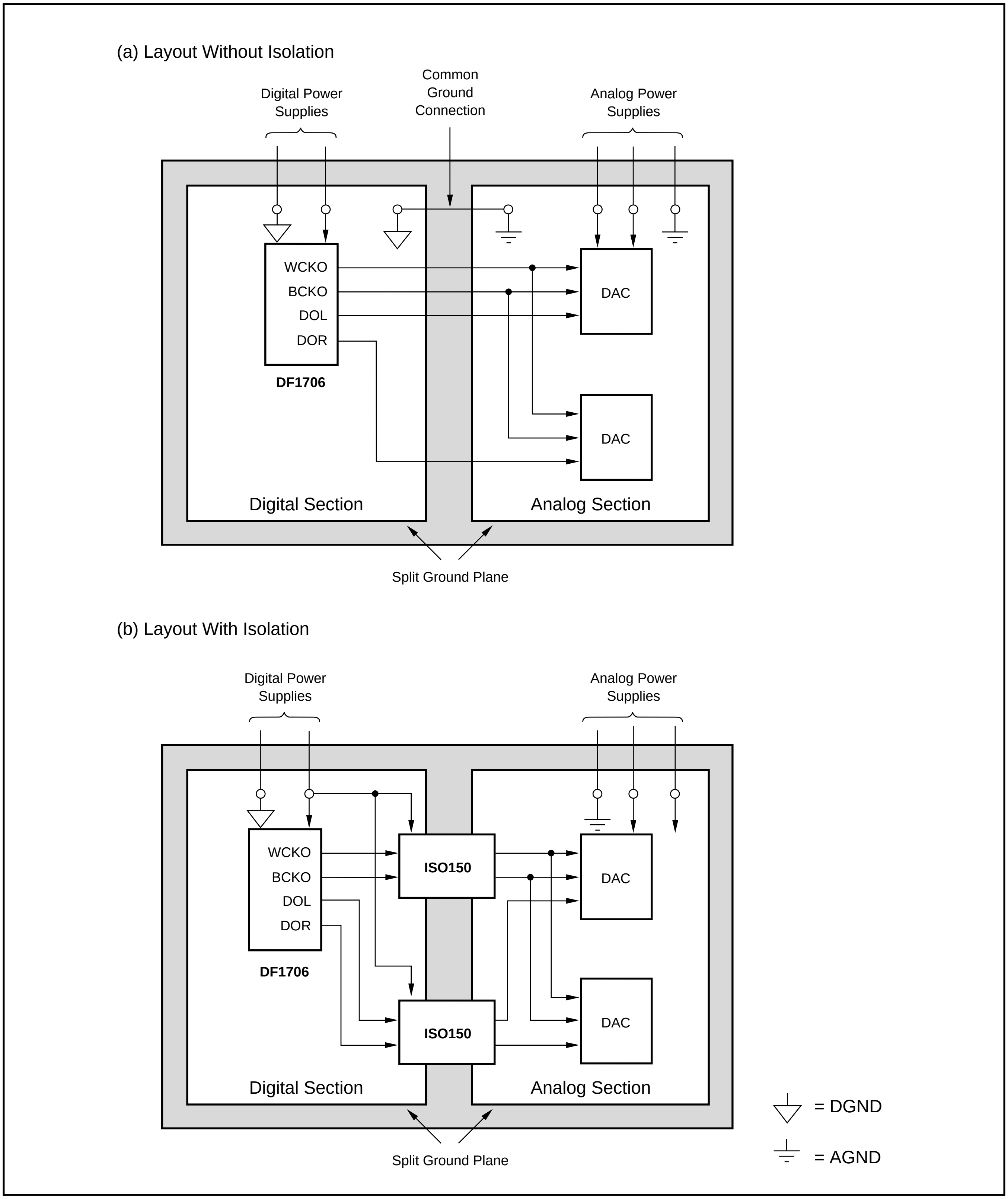


FIGURE 11. PCB Layout Model.

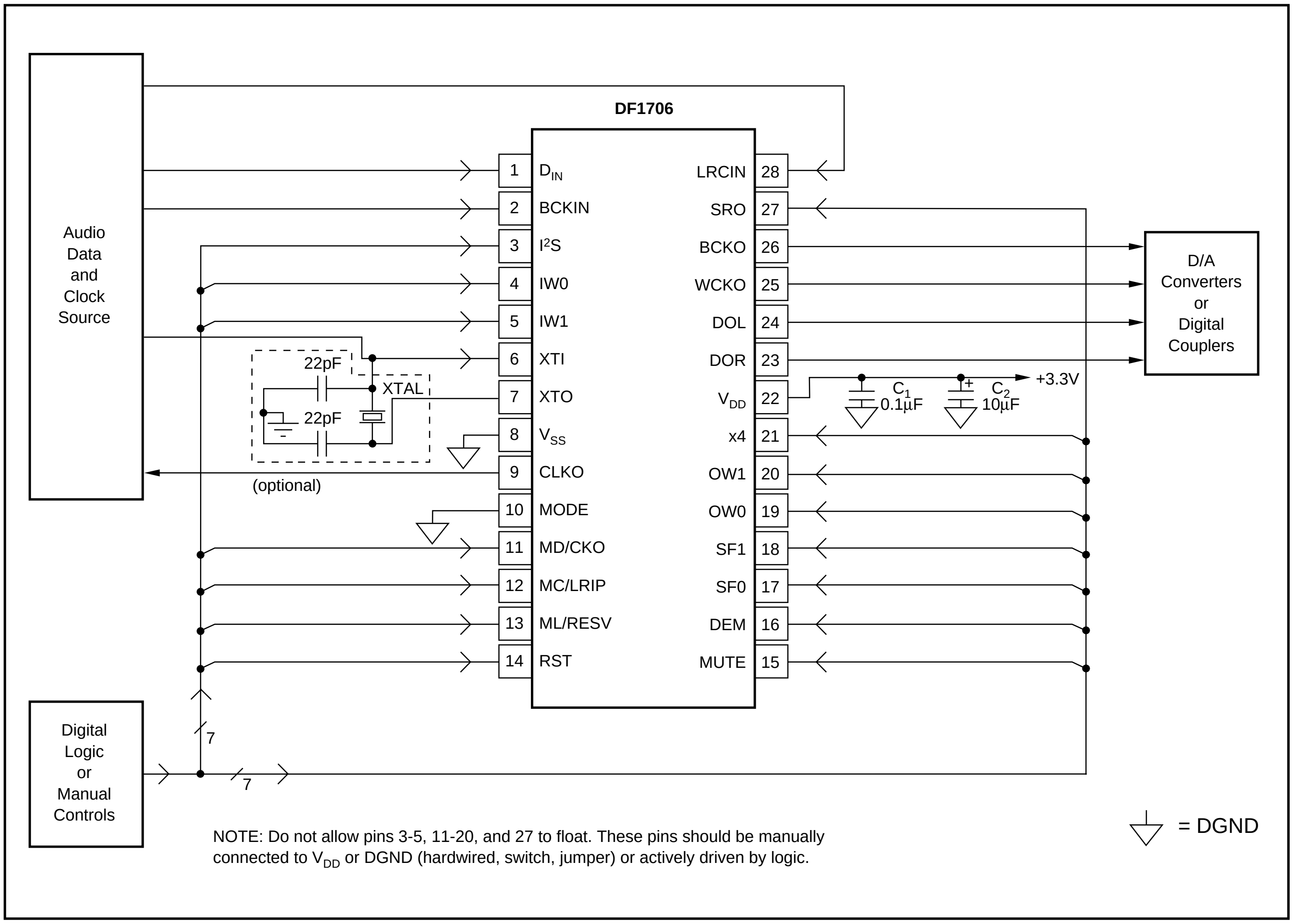


FIGURE 12. Basic Circuit Connections, Hardware Control.

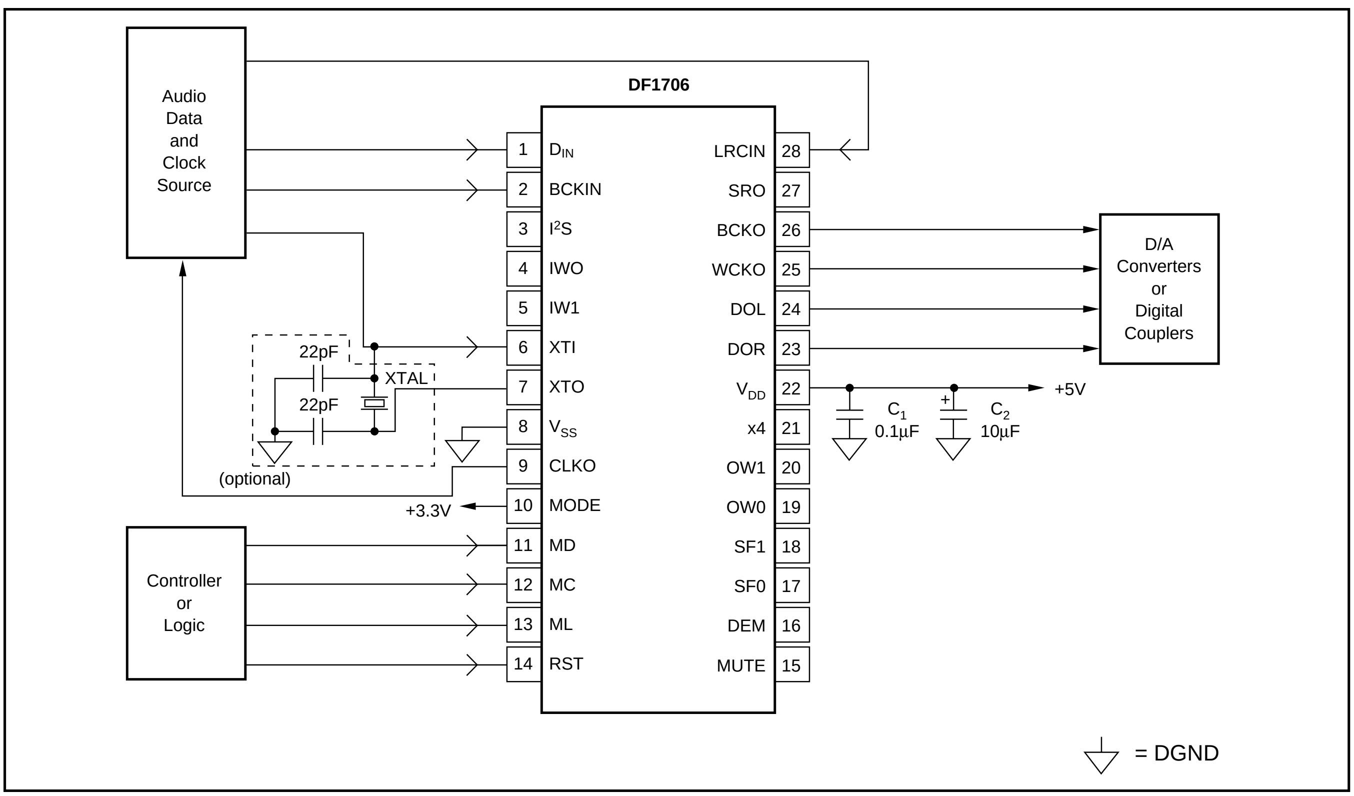


FIGURE 13. Basic Circuit Connection, Software Control.

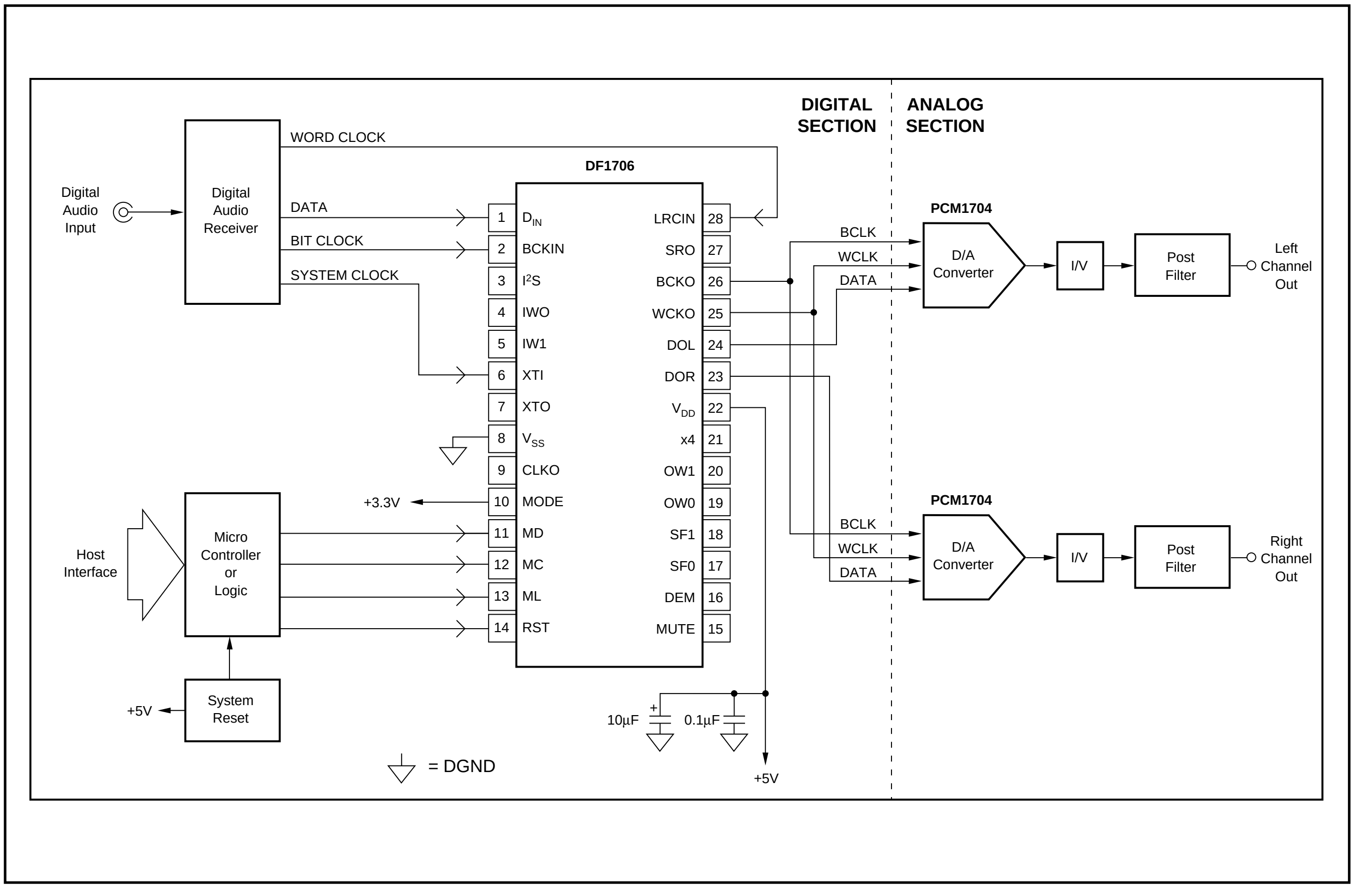


FIGURE 14. DF1706 Typical Application Circuit.

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